IN THE CLAIMS:

Claims 4, 9-13, 30, 35-39, 42, 44-48, 52, 57-61, 78, 83-87, 90, 92-96, 100, 105-109 and 117-136 have been canceled. Claims 1, 5 and 6 have been amended herein. All of the pending claims 1 through 136 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

**Listing of Claims:**

1. (currently amended) A semiconductor device assembly comprising:

a substrate having a surface, having a first passivation layer provided over at least a portion of said surface of said substrate, having a second passivation layer provided over at least a portion of said first passivation layer, having a layer comprising substantially diamond provided over at least a portion of said second passivation layer having at least one aperture therein, and having at least one contact pad having a periphery, said at least one contact pad having at least a portion thereof extending at least partially over said layer comprising substantially diamond adjacent said at least one aperture therein and having at least a portion thereof extending through said at least one aperture in said layer comprising substantially diamond connected to at least one circuit on said substrate.

2. (previously presented) The assembly according to claim 1, wherein said periphery of said at least one contact pad covers portions of said layer comprising substantially diamond adjacent said at least one aperture therein.

3. (original) The assembly according to claim 1, further comprising a conductive bump deposited on said at least one contact pad.

4. (canceled)

5. (currently amended) The assembly according to claim 1, wherein at least one of said first passivation layer and said second passivation layer has at least one trace having at least a portion thereof located on a portion of at least one of said first passivation layer and said second passivation layer to connect said substrate and said at least one contact pad.

6. (currently amended) The assembly according to claim 1, wherein said first passivation layer and said second passivation layer comprise a polyimide.

7. (previously presented) The assembly according to claim 1, wherein said layer comprising substantially diamond has a thickness of at least about 50 angstroms.

8. (previously presented) The assembly according to claim 1, wherein said layer comprising substantially diamond has a thickness of between about 50 and 2000 angstroms.

9-13. (canceled)

14. (original) The assembly according to claim 1, wherein said layer comprising substantially diamond comprises substantially polycrystalline diamond.

15. (original) The assembly according to claim 1, wherein said layer comprising substantially diamond comprises substantially amorphous diamond.

16. (original) The assembly according to claim 1, wherein said layer comprising substantially diamond comprises polycrystalline diamond and amorphous diamond.

17. (previously presented) The assembly according to claim 1, wherein said layer comprising substantially diamond includes one of polycrystalline diamond, amorphous diamond and another material.

18. (previously presented) The assembly according to claim 1, wherein said layer comprising substantially diamond includes polycrystalline diamond, amorphous diamond and another material.

19. (original) The assembly according to claim 1, wherein said substrate comprises: a semiconductor die.

20. (original) The assembly according to claim 1, wherein said substrate comprises: a bare semiconductor die.

21. (original) The assembly according to claim 1, wherein said substrate comprises: a semiconductor wafer.

22. (original) The assembly according to claim 1, wherein said substrate comprises: a portion of a semiconductor wafer.

23. (original) The assembly according to claim 1, wherein said substrate comprises: a carrier substrate.

24. (original) The assembly according to claim 1, wherein said substrate comprises: a carrier substrate for a flip-chip semiconductor device assembly.

25. (original) The assembly according to claim 1, wherein said substrate comprises: a carrier substrate having a semiconductor die attached thereto.

26. (original) The assembly according to claim 1, wherein said substrate comprises: a carrier substrate having a semiconductor die adhesively attached thereto.

27. (previously presented) A semiconductor die assembly comprising:
a substrate having a surface, a passivation layer, said passivation layer provided over at least a portion of said surface of said substrate, a second passivation layer, said second passivation layer provided over said passivation layer, a layer including diamond having at least one aperture therein, said layer provided substantially over said second passivation layer, and at least one contact pad having at least a portion thereof extending at least partially over said layer and having a portion thereof extending at least into said at least one aperture in said layer.

28. (original) The assembly according to claim 27, wherein said at least one contact pad has substantially a periphery thereof contacting said layer.

29. (original) The assembly according to claim 27, further comprising:
a conductive bump located on said at least one contact pad.

30. (canceled)

31. (previously presented) The assembly according to claim 27, wherein at least one of said passivation layer and said second passivation layer carries at least one trace to electrically connect said substrate and said at least one contact pad.

32. (previously presented) The assembly according to claim 27, wherein said passivation layer and said second passivation layer comprise a polyimide.

33. (original) The assembly according to claim 27, wherein said layer has a thickness of at least about 50 angstroms.

34. (previously presented) The assembly according to claim 27, wherein said layer has a thickness of between about 50 and 2000 angstroms.

35-39. (canceled)

40. (previously presented) A heat sink disposed on a substrate comprising:
a passivation layer disposed on at least a portion of a surface of a substrate;
a second passivation layer disposed on at least a portion of said passivation layer;
a layer including diamond disposed on at least a portion of said second passivation layer, said layer including at least one opening therein; and
at least one pad located on at least a portion of said surface of said substrate, said at least one pad having a portion thereof extending over at least a portion of said layer and having a portion thereof located in said at least one opening.

41. (previously presented) The heat sink according to claim 40, wherein said at least one pad has more than one portion thereof extending over said at least said portion of said layer.

42. (canceled)

43. (previously presented) The heat sink according to claim 40, wherein at least one of said passivation layer and said second passivation layer has at least one trace connecting said substrate and said at least one pad.

44-48. (canceled)

49. (previously presented) A semiconductor device assembly comprising:
a semiconductor device having an active surface, having a passivation layer provided over at least a portion of said active surface of said semiconductor device, having a second passivation layer provided over at least a portion of said passivation layer, having a layer comprising substantially diamond provided over at least a portion of said second passivation layer having at least one aperture therein, and having at least one bond pad having a periphery located on said active surface, said at least one bond pad having at least a portion thereof extending at least partially over said layer comprising substantially diamond adjacent said at least one aperture therein and having at least a portion thereof extending at least through a portion of said at least one aperture in said layer comprising substantially diamond, said at least one bond pad connected to at least one circuit on said semiconductor device; and
a substrate.

50. (previously presented) The assembly according to claim 49, wherein said periphery of said at least one bond pad covers portions of said layer adjacent said at least one aperture therein.

51. (original) The assembly according to claim 49, further comprising:
a conductive bump deposited on said at least one bond pad.

52. (canceled)

53. (previously presented) The assembly according to claim 49, wherein at least one of said passivation layer and said second passivation layer has at least one trace having at least a portion thereof located on a portion of at least one of said passivation layer and said second passivation layer to connect said semiconductor device and said at least one bond pad.

54. (previously presented) The assembly according to claim 49, wherein said passivation layer and said second passivation layer comprise a polyimide.

55. (original) The assembly according to claim 49, wherein said layer comprising substantially diamond has a thickness of at least about 50 angstroms.

56. (previously presented) The assembly according to claim 49, wherein said layer comprising substantially diamond has a thickness of between about 50 and 2000 angstroms.

57-61. (canceled)

62. (original) The assembly according to claim 49, wherein said layer comprising substantially diamond comprises substantially polycrystalline diamond.

63. (original) The assembly according to claim 49, wherein said layer comprising substantially diamond comprises substantially amorphous diamond.

64. (original) The assembly according to claim 49, wherein said layer comprising substantially diamond comprises polycrystalline diamond and amorphous diamond.

65. (original) The assembly according to claim 49, wherein said layer comprising substantially diamond includes one of polycrystalline diamond, amorphous diamond, and another material.

66. (previously presented) The assembly according to claim 49, wherein said layer comprising substantially diamond includes polycrystalline diamond, amorphous diamond and another material.

67. (original) The assembly according to claim 49, wherein said semiconductor device comprises:
a semiconductor die.

68. (original) The assembly according to claim 49, wherein said semiconductor device comprises:
a bare semiconductor die.

69. (original) The assembly according to claim 49, wherein said semiconductor device comprises:
a semiconductor wafer.

70. (original) The assembly according to claim 49, wherein said semiconductor device comprises:
a portion of a semiconductor wafer.

71. (original) The assembly according to claim 49, wherein said semiconductor device comprises:
a flip-chip semiconductor die.

72. (original) The assembly according to claim 49, wherein said substrate comprises:
a carrier substrate for a flip-chip semiconductor device assembly.

73. (original) The assembly according to claim 49, wherein said substrate comprises:
a carrier substrate having a semiconductor die attached thereto.

74. (original) The assembly according to claim 67, wherein said substrate comprises:
a carrier substrate having said semiconductor die adhesively attached thereto.

75. (previously presented) A semiconductor die assembly comprising:

a semiconductor die having an active surface, a passivation layer, said passivation layer provided substantially over a portion of said active surface of said semiconductor device, a second passivation layer, said second passivation layer provided substantially over a apportion of said passivation layer, a layer having at least one aperture therein, said layer including diamond provided substantially over a portion of said second passivation layer, and at least one bond pad having at least a portion thereof extending at least partially over said layer and having a portion thereof extending at least into said at least one aperture in said layer; and

a substrate having said semiconductor die attached thereto.

76. (original) The assembly according to claim 75, wherein said at least one bond pad has substantially a periphery thereof contacting said layer.

77. (original) The assembly according to claim 75, further comprising:

a conductive bump located on said at least one bond pad.

78. (canceled)

79. (previously presented) The assembly according to claim 75, wherein at least one of said passivation layer and said second passivation layer has at least one trace connecting said semiconductor die and said at least one bond pad.

80. (previously presented) The assembly according to claim 75, wherein said passivation layer and said second passivation layer comprise a polyimide.

81. (original) The assembly according to claim 75, wherein said layer has a thickness of at least about 50 angstroms.

82. (previously presented) The assembly according to claim 75, wherein said layer has a thickness of between about 50 and 2000 angstroms.

83-87. (canceled)

88. (previously presented) A heat sink disposed on a semiconductor device comprising:

a passivation layer disposed on at least a portion of an active surface of a semiconductor device;

a second passivation layer disposed on at least a portion of said passivation layer;

a layer including diamond disposed on at least a portion of said second passivation layer, said layer including at least one opening therein; and

at least one bond pad located on at least a portion of said active surface of said semiconductor device, said at least one bond pad having a portion thereof extending over at least a portion of said layer and having another portion thereof located in said at least one opening.

89. (previously presented) The heat sink according to claim 88, wherein said at least one bond pad has more than one portion thereof extending over said at least a portion of said layer.

90. (canceled)

91. (previously presented) The heat sink according to claim 88, wherein at least one of said passivation layer and said second passivation layer has at least one trace connecting said semiconductor device and said at least one bond pad.

92-96. (canceled)

97. (previously presented) A semiconductor die comprising:

a substrate having a surface, at least one circuit located on said substrate, a passivation layer provided over at least a portion of said surface of said substrate, a second passivation layer provided over at least a portion of said passivation layer, a layer including diamond provided over at least a portion of said second passivation layer having at least one aperture therein, and having at least one contact pad having a periphery, said at least one contact pad having at least a portion thereof extending at least partially over said layer adjacent said at least one aperture therein and having at least a portion thereof extending through said at least one aperture in said layer, said at least one contact pad connected to said at least one circuit on said substrate.

98. (previously presented) The semiconductor die according to claim 97, wherein said periphery of said at least one contact pad covers portions of said layer adjacent said at least one aperture therein.

99. (original) The semiconductor die according to claim 97, further comprising:

a conductive bump deposited on said at least one contact pad.

100. (canceled)

101. (previously presented) The semiconductor die according to claim 97, wherein at least one of said passivation layer and said second passivation layer has at least one trace having at least a portion thereof located on a portion of at least one of said passivation layer and said second passivation layer to connect said substrate and said at least one contact pad.

102. (previously presented) The semiconductor die according to claim 97, wherein said passivation layer and said second passivation layer comprise a polyimide.

103. (original) The semiconductor die according to claim 97, wherein said layer has a thickness of at least about 50 angstroms.

104. (original) The semiconductor die according to claim 97, wherein said layer has a thickness of between about 50 and 2000 angstroms.

105-109. (canceled)

110. (original) The semiconductor die according to claim 97, wherein said layer comprises substantially polycrystalline diamond.

111. (original) The semiconductor die according to claim 97, wherein said layer comprises substantially amorphous diamond.

112. (original) The semiconductor die according to claim 97, wherein said layer comprises polycrystalline diamond and amorphous diamond.

113. (previously presented) The semiconductor die according to claim 97, wherein said layer includes one of polycrystalline diamond, amorphous diamond and another material.

114. (previously presented) The semiconductor die according to claim 97, wherein said layer includes polycrystalline diamond, amorphous diamond and another material.

115. (original) The semiconductor die according to claim 97, wherein said substrate comprises:
a semiconductor wafer.

116. (original) The semiconductor die according to claim 97, wherein said substrate comprises:
a portion of a semiconductor wafer.

117-136. (canceled)